

155

(19) World Intellectual Property Organization
International Bureau



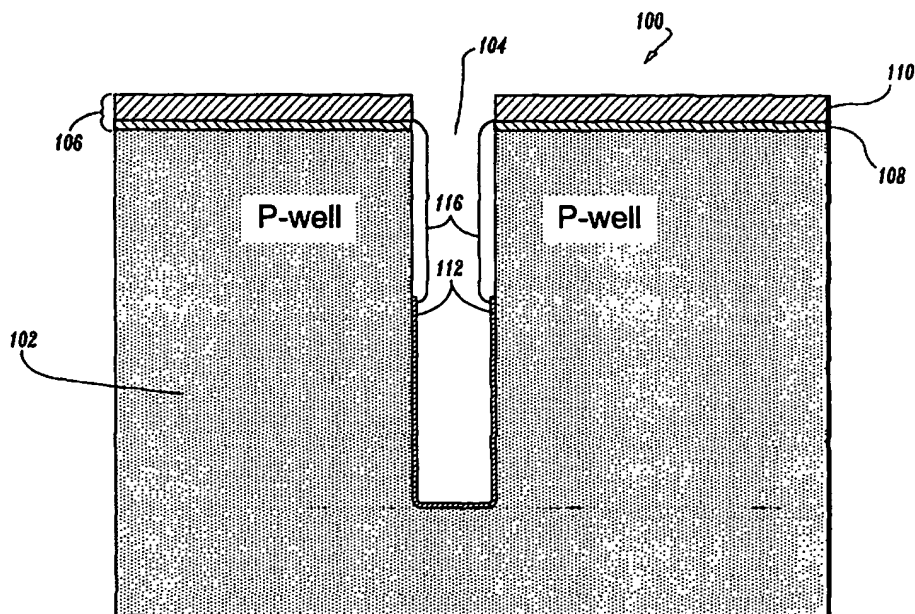
(43) International Publication Date
27 December 2001 (27.12.2001)

PCT

(10) International Publication Number
WO 01/99158 A2

- (51) International Patent Classification⁷: **H01L 21/00** **SPINDLER, Oswald**; Lortzingstrasse 16, 85591 Vaterstetten (DE). **GABRIC, Zvonimir**; Herzog-Rudolf Weg 25, 85604 Zorneding (DE).
- (21) International Application Number: **PCT/US01/19578**
- (22) International Filing Date: **19 June 2001 (19.06.2001)** (74) Agents: **BRADEN, Stanton, C. et al.**; Siemens Corporation, Intellectual Property Dept., 186 Wood Avenue South, Iselin, NJ 08830 (US).
- (25) Filing Language: **English**
- (26) Publication Language: **English** (81) Designated States (national): **JP, KR.**
- (30) Priority Data: **09/596,606** **19 June 2000 (19.06.2000)** **US** (84) Designated States (regional): **European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR).**
- (71) Applicant: **INFINEON TECHNOLOGIES NORTH AMERICA CORP.** [US/US]; 1730 North First Street, San Jose, CA 95112-4508 (US). Published:
— *without international search report and to be republished upon receipt of that report*
- (72) Inventors: **BEINTNER, Jochen**; 27 Clapp Avenue, Wappingers Falls, NY 12590 (US). **MICHAELIS, Alexander**; Grundermuehlenweg 38, 51381 Leverkusen (DE). **GRUENING, Ulrike**; Raintalerstr. 36, 81539 Munich (DE). *For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.*

(54) Title: **COLLAR FORMATION BY SELECTIVE OXIDE DEPOSITION**



(57) Abstract: A method for forming an oxide collar in a trench, in accordance with the present invention, includes forming a trench (104) in a silicon substrate (102), and depositing and recessing a nitride liner (112) in the trench to expose a portion of the silicon substrate on sidewalls of the trench. An oxide (116) is deposited selective to the nitride liner on the portion of the silicon substrate. Residue oxide is removed from surfaces of the nitride liner to form a collar (116) in the trench.



WO 01/99158 A2

COLLAR FORMATION BY SELECTIVE OXIDE DEPOSITIONBACKGROUND1. Technical Field

This disclosure relates to semiconductor fabrication and more particularly, to a method for forming an oxide collar in a deep trench by employing a selective oxide deposition.

2. Description of the Related Art

Semiconductor memory devices, for example, dynamic random access memories (DRAM=s), include capacitors to store data which are accessed by transistors (e.g., access transistors). Deep trench (DT) capacitors are among the types of capacitors employed in DRAM technology. Deep trench capacitors are typically buried within a semiconductor substrate. In the case of a p-type doped Si-substrate, a bottom portion of the trenches has to be n-type doped to form a buried plate (e.g., one electrode of the capacitor). This buried plate is separated from the n-type doped source region of the access transistor by a p-type doped substrate region. Consequently, there is an n/p/n junction along the vertical side of the DT.

The n/p/n junction forms a transistor by itself. This undesired transistor is called a vertical device or a parasitic device and may cause a severe leakage of charge from the buried plate to the access transistor if it is turned on. To prevent this vertical leakage, a thick dielectric layer is formed along the n/p/n junction. This dielectric layer is

called the trench collar and conventionally includes SiO_2 . This oxide collar has the same function as a gate oxide of the access transistor. The thickness of the collar oxide determines the threshold voltage V_t of the parasitic device. Once the applied voltage is larger than V_t , the transistor is turned on and charge can detrimentally flow through the n/p/n junction. This should be avoided in the vertical device, i.e. the oxide collar thickness must be large enough that the vertical device never turns on during DRAM operation.

Conventionally voltages in the order of $V_D/2$ are applied to the DT where V_D is the power supply voltage (typically, about 3 V). To prevent the vertical device from turning on a collar oxide thickness above about 25 nm is needed. Currently this collar oxide is formed by a chemical vapor deposition (CVD) or a physical vapor deposition (PVD) with a subsequent collar open etch. Alternately, a LOCOS process (localized oxidation of silicon) may be employed. The LOCOS process permits for an easier (cheaper) process integration flow if compared to the PVD/CVD processes and is more suitable for smaller ground rules (for a better trench profile). However, the conventional LOCOS collar has the following drawbacks:

- 1) The LOCOS oxide thickness shows a severe dependence on the Si-crystal orientation of the semiconductor substrate resulting in a non-uniform collar with thin regions. In the thin regions V_t drops significantly causing reliability problems.

2) The trench opening (CD) for the LOCOS collar has to be reduced as the collar oxidation consumes silicon of the substrate.

3) To prevent oxidation of the trench sidewalls a nitride liner is needed in the bottom part of the trench where no oxide is to be formed. In case of the conventional LOCOS process, this liner has to be thicker than 5 or 6 nm to prevent oxidation of the Si interface. This thick layer is difficult to remove.

Therefore, a need exists for methods, which overcome the disadvantages of the prior art. A further need exists for a selective deposition process, which forms an oxide collar selectively on silicon.

SUMMARY OF THE INVENTION

A method for forming an oxide collar in a trench, in accordance with the present invention, includes forming a trench in a silicon substrate, and depositing and recessing a nitride liner in the trench to expose a portion of the silicon substrate on sidewalls of the trench. An oxide is deposited selective to the nitride liner on the portion of the silicon substrate. Residue oxide is removed from surfaces of the nitride liner to form a collar in the trench.

In other methods, the step of depositing an oxide selective to the nitride liner on the portion of the silicon substrate may include the step of depositing an ozone activated tetraethyl orthosilicate (TEOS) oxide selective to

the nitride liner on the portion of the silicon substrate. The step of depositing an ozone activated tetraethyl orthosilicate (TEOS) oxide selective to the nitride liner on the portion of the silicon substrate may include the step of providing an initial gas flow ratio of TEOS to ozone of approximately 10 and attaining a steady-state gas flow ratio of TEOS to ozone of 0.4. The step of etching residue oxide from surfaces of the nitride liner to form a collar in the trench may include the step of wet etching the residue oxide. The step of depositing and recessing a nitride liner may include the steps of filling the trench with a resist over the nitride liner, recessing the resist to expose a portion of the nitride liner and etching the nitride liner to a top level of the resist in the trench to expose the portion of the substrate in the trench. The nitride liner may be between about 2 nm and 3 nm in thickness. The method further includes the step of forming a buried plate adjacent to a lower portion of the trench. The method may include the step of annealing the oxide.

A method for forming an oxide collar in a trench, in accordance with the present invention, includes the steps of forming a trench in a silicon substrate, depositing a nitride liner in the trench, and recessing the nitride liner to expose a portion of the silicon substrate on sidewalls of the trench. An ozone activated tetraethyl orthosilicate (TEOS) oxide is deposited selective to the nitride liner on the portion of the

silicon substrate. The oxide is substantially homogenous in thickness such that the thickness of the oxide is independent of a crystallographic orientation of the portion of the substrate on which the oxide is formed. Residue oxide is etched from surfaces of the nitride liner to form a collar in the trench.

The step of depositing an ozone activated tetraethyl orthosilicate (TEOS) oxide may include the step of providing an initial gas flow ratio of TEOS to ozone of approximately 10 and attaining a steady-state gas flow ratio of TEOS to ozone of 0.4. The step of etching residue oxide from surfaces of the nitride liner to form a collar in the trench may include the step of wet etching the residue oxide. The step of recessing a nitride liner may include the steps of filling the trench with a resist over the nitride liner, recessing the resist to expose a portion of the nitride liner and etching the nitride liner to a top level of the resist in the trench to expose the portion of the substrate in the trench. The nitride liner may be between about 2 nm and 3 nm in thickness.

The method may include the step of forming a buried plate adjacent to a lower portion of the trench. The method may further include the step of annealing the oxide.

These and other objects, features and advantages of the present invention will become apparent from the following detailed description of illustrative embodiments thereof,

which is to be read in connection with the accompanying drawings.

BRIEF DESCRIPTION OF DRAWINGS

This disclosure will present in detail the following description of preferred embodiments with reference to the following figures wherein:

FIG. 1 is a flow diagram showing a method for selectively depositing an oxide collar in a deep trench in accordance with the present invention;

FIG. 2 is a cross-sectional view of a trench having a selectively deposited oxide formed therein in accordance with the present invention; and

FIG. 3 is a cross-sectional view of the selectively deposited oxide etched to form the collar in accordance with the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

The present invention provides methods for selectively forming an oxide collar on silicon surfaces of a deep trench.

In a preferred embodiment, a selective TEOS-Ozone deposition process is employed in which an oxide forms on a silicon surface selective to nitride. The disclosed methods permit a uniform, low temperature collar oxide formation including at least the following advantages with respect to the conventional LOCOS collar process:

- 1) No dependence of oxide thickness on Si-crystal orientation (reliability);

- 2) No consumption of trench silicon (higher value for CD);
- 3) Uniform oxide deposition (no birds beak effects or thinning in particular areas); and
- 4) No silicon nitride consumption during deposition.

These advantages will become clear from the following description and the accompanying FIGs. It is to be understood that the present invention is described in terms of an ozone assisted TEOS deposition process; however, the invention is broader and is applicable to any selective oxide deposition process. The present invention is not to be construed as limited by the examples described herein. Instead, the examples set forth herein are illustrative.

Referring now in specific detail to the drawings in which like reference numerals identify similar or identical elements throughout the several views, and initially to FIG. 1, a flow diagram is shown for a method of forming a dielectric collar by employing a selective oxide deposition process. In block 10, a deep trench is formed in a mono-crystalline substrate. A masking layer, which may include a hard mask, of, for example a silicate glass, is patterned over a pad stack (which is formed on the substrate). The substrate is etched, for example, by a reactive ion etch process, to form a deep trench in accordance with the patterned hard mask. In block 12, a buried plate may be formed in a bottom portion of the trench. The buried plate may be formed before or after a collar is

formed in the trench in accordance with block 20. Formation of the buried plate may be performed by employing an arsenic silicate glass (ASG) drive in process, known in the art. Alternatively, the buried plate formation can be performed after collar formation, in block 20, by a self aligned ASG process, gas phase or plasma doping.

In block 14, a liner nitride, e.g., silicon nitride, is deposited in the trench. Advantageously, a thin layer of nitride is employed, which makes the nitride easier to remove from the sidewalls of the trench. In a preferred embodiment, a nitride liner of between about 2 nm and about 3 nm is employed, and more preferably about 2.5 nm. Thicker nitrides may be employed as well. In block 16, a resist fill and recess are performed to fill the trench and then recess the resist below the level of a p-well formed adjacent to the trench. P-wells are known in the art. This recess step exposes a portion of the nitride liner, which is to be removed to expose the substrate along a portion of sidewalls of the trench. In block 18, removal of the exposed nitride liner is performed by employing an etch process, such as, for example, a dry or wet etching process, preferably selective to the resist which fills a portion of the trench. The nitride liner is removed from an area where the oxide collar will be formed. By removing the thin nitride liner the bare Si-surface is exposed. The resist is now stripped to remove it from the trench.

In block 20, a selective collar deposition process is employed to form an oxide on the exposed Si with little or no deposition of the exposed nitride liner remaining in the trench or on a nitride layer of the pad stack. The oxide formed on the exposed Si substrate (sidewalls of the trench) forms the oxide collar. In a preferred embodiment, a TEOS-Ozone oxide deposition is employed.

The ozone activated deposition is performed in a chemical vapor deposition apparatus, which is modified to provide ozone activated TEOS. The growth of TEOS in accordance with this process is selective to the exposed silicon surfaces. Significantly, less TEOS growth occurs on the nitride liner (less than about 1/5 of the growth on bare silicon). In a preferred embodiment, the ozone activated TEOS is grown by employing a gas phase deposition process.

In preferred embodiments, the TEOS-ozone layer attains a very homogeneous silicon oxide layer without fluctuations in stoichiometry by providing that at the beginning of a gas phase deposition, a gas flow ratio of TEOS to ozone is very high and subsequently is varied until a steady-state ratio is attained, in which the gas flow ratio of TEOS to ozone is low.

In an exemplary embodiment, the initial gas flow ratio of TEOS to the ozone-containing gas is approximately 10, while in the case of the steady-state gas flow ratio attained after approximately one and a half minutes, the value of 0.4 is attained.

Beginning with the initial gas flow ratio, it is advantageous initially to keep the TEOS gas flow constant and to increase the ozone gas flow. While, subsequently, the ozone gas flow is increased further up to its steady-state final value, the TEOS gas flow can be reduced down to its steady-state final value. The variation is, therefore, preferably effected nonlinearly, although a linear variation of the ratio is also possible.

By increasing the ozone (or ozone containing gas) gas flow, which is produced with an ozone generator, the proportion of oxygen in the entire gas flow also decreases simultaneously during this starting phase. This is shown in a first column of a table shown below with process parameters of an exemplary embodiment, while second and third columns indicate the gas flow of the ozone and TEOS, respectively. At a largely constant O_2 / O_3 gas flow, the ratio of these two gases therefore varies from a low proportion of ozone to a high proportion of ozone.

The variation in the ratio of the initial gas flow conditions to the steady-state gas flow conditions is preferably carried out continuously, although in actual practice, it is performed in stages over time. To improve the conditions needed for desensitization of the deposition process, the initial gas flow ratio of TEOS to ozone is initially varied slowly, but then comparatively quickly until the steady-state final value. While the entire starting

process until the steady-state final value is reached lasts about one and a half minutes, for about half of this total time the initial TEOS total flow is still constant, while the ozone-containing gas flow amounts to about two and a half times the initial value.

Overall, the ratio of the gas flows of TEOS to ozone, at this point, is approximately four. As a result of the contrary variations in the TEOS gas flow and the ozone gas flow that then ensue, the TEOS gas flow at the end of the starting process is reduced to about two-thirds of its initial value, while the ozone flow amounts to more than 15 times the initial gas flow.

The table below provides a survey of possible exemplary process parameters. Parameters, which are not listed, such as pressure and temperature, match those of a known standard process, for example, being approximately 600 Torr and approximately 400°C.

Time	O ₂ sccm*	O ₃ sccm*	TEOS sccm*
15"	5000	300	3000
11"	5000	500	3000
18"	5000	750	3000
15"	5000	1000	2800
12"	4000	2000	2600
9"	3000	3000	2400
6"	2000	4000	2200
3"	1000	5000	2000
X"	--	5000	2000

*sccm = standard cm³ of gas flow

Other selective oxide formation processes may also be employed.

Referring to FIG. 2, a cross-sectional view of a partially fabricated trench capacitor cell 100 is shown in accordance with the present invention. Cell 100 includes a substrate 102 having a deep trench 104 formed therein. A pad stack 106 is formed on substrate 102. Pad stack 106 preferably includes an oxide layer 108, for example, a thermal oxide and a nitride layer 110 (e.g., silicon nitride). Trench 104 includes a nitride liner 112 which lines a lower portion of trench 104. Liner 112 is preferably formed as described above. A selectively deposited oxide layer 114 is shown for forming a collar 116 (see FIG. 3) in accordance with the present invention. Layer 114 is thicker on bare silicon regions 118 than on liner 112 and nitride layer 110 of pad stack 106. Layer 114 is preferably formed by employing an ozone activated TEOS process.

By employing such a process, the thickness of nitride liner 112 is advantageously reduced without risk of oxidizing substrate 102 through liner 112. The thinner liner 112 also provides easier removal hence maintaining the critical dimension (CD) of the opening of trench 104 (relieves excessive etching). Selective oxide deposition processes preferably employ lower temperatures for deposition, lower than for example, LOCOS processes. Temperatures in the range of between about 350°C to about 600°C, and more preferably

between about 350°C to about 450°C, and thereby conserve the thermal budget for the fabrication process. A buried plate 121 is illustratively shown.

Returning to FIG. 1, in block 22, an optional post anneal of the selectively deposited oxide is performed. This post anneal process, if performed, is preferably in the temperature range between 700°C and 1000°C in an inert or oxidizing ambient. The post anneal process may be performed to densify the collar. In block 24, an etching process removes the selectively deposited oxide from the pad stack and the nitride liner. The etching process preferably includes a wet etch, for example, employing HF, or diluted HF or a dry etch. The buried plate may now be formed, if not formed previously, and processing continues as is known in the art.

Referring to FIG. 3, a cross-sectional view of cell 100 is shown after the etch back of the selectively deposited oxide. A collar 116 is formed, which is advantageously self-aligned to the exposed silicon of the sidewalls of trench 104 in substrate 102, since collar 116 is formed by a selective TEOS-Ozone deposition process in which the oxide is deposited selective to silicon nitride. Collar 116 is uniform in thickness (e.g., includes a thickness variation of less than about 5-7%, and is virtually independent of crystallographic orientations of the substrate 102.

The disclosed processes include at least the following advantages over the high temperature LOCOS collar formation:

1) Improved collar oxide thickness homogeneity resulting in more reliable oxides (no dependence of oxide thickness on Si-crystal orientation);

2) High selectivity to nitride liner permits thinner masking layers (easy nitride strip);

3) Low temperature;

4) Trench opening not significantly etched in removing the nitride liner; and

5) Silicon nitride is not consumed during deposition.

Having described preferred embodiments for collar formation by selective oxide deposition (which are intended to be illustrative and not limiting), it is noted that modifications and variations can be made by persons skilled in the art in light of the above teachings. It is therefore to be understood that changes may be made in the particular embodiments of the invention disclosed which are within the scope and spirit of the invention as outlined by the appended claims. Having thus described the invention with the details and particularity required by the patent laws, what is claimed and desired protected by Letters Patent is set forth in the appended claims.

WHAT IS CLAIMED IS:

1. A method for forming an oxide collar in a trench, comprising the steps of:
 - forming a trench in a silicon substrate;
 - depositing and recessing a nitride liner in the trench to expose a portion of the silicon substrate on sidewalls of the trench;
 - depositing an oxide selective to the nitride liner on the portion of the silicon substrate; and
 - etching residue oxide from surfaces of the nitride liner to form a collar in the trench.
2. The method as recited in claim 1, wherein the step of depositing an oxide selective to the nitride liner on the portion of the silicon substrate includes the step of depositing an ozone activated tetraethyl orthosilicate (TEOS) oxide selective to the nitride liner on the portion of the silicon substrate.
3. The method as recited in claim 1, wherein the step of depositing an ozone activated tetraethyl orthosilicate (TEOS) oxide selective to the nitride liner on the portion of the silicon substrate includes the step of providing an initial gas flow ratio of TEOS to ozone of approximately 10 and attaining a steady-state gas flow ratio of TEOS to ozone of 0.4.
4. The method as recited in claim 1, wherein the step of etching residue oxide from surfaces of the nitride

liner to form a collar in the trench includes the step of wet etching the residue oxide.

5. The method as recited in claim 1, wherein the step of depositing and recessing a nitride liner includes the steps of:

filling the trench with a resist over the nitride liner;

recessing the resist to expose a portion of the nitride liner; and

etching the nitride liner to a top level of the resist in the trench to expose the portion of the substrate in the trench.

6. The method as recited in claim 1, wherein the nitride liner is between about 2 nm and 3 nm in thickness.

7. The method as recited in claim 1, further comprising the step of forming a buried plate adjacent to a lower portion of the trench.

8. The method as recited in claim 1, further comprising the step of annealing the oxide.

9. A method for forming an oxide collar in a trench, comprising the steps of:

forming a trench in a silicon substrate;

depositing a nitride liner in the trench;

recessing the nitride liner to expose a portion of the silicon substrate on sidewalls of the trench;

depositing an ozone activated tetraethyl orthosilicate (TEOS) oxide selective to the nitride liner on the portion of the silicon substrate, the oxide being substantially homogenous in thickness such that the thickness of the oxide is independent of a crystallographic orientation of the portion of the substrate on which the oxide is formed; and

etching residue oxide from surfaces of the nitride liner to form a collar in the trench.

10. The method as recited in claim 9, wherein the step of depositing an ozone activated tetraethyl orthosilicate (TEOS) oxide includes the step of providing an initial gas flow ratio of TEOS to ozone of approximately 10 and attaining a steady-state gas flow ratio of TEOS to ozone of 0.4.

11. The method as recited in claim 9, wherein the step of etching residue oxide from surfaces of the nitride liner to form a collar in the trench includes the step of wet etching the residue oxide.

12. The method as recited in claim 9, wherein the step of recessing a nitride liner includes the steps of:

filling the trench with a resist over the nitride liner;

recessing the resist to expose a portion of the nitride liner; and

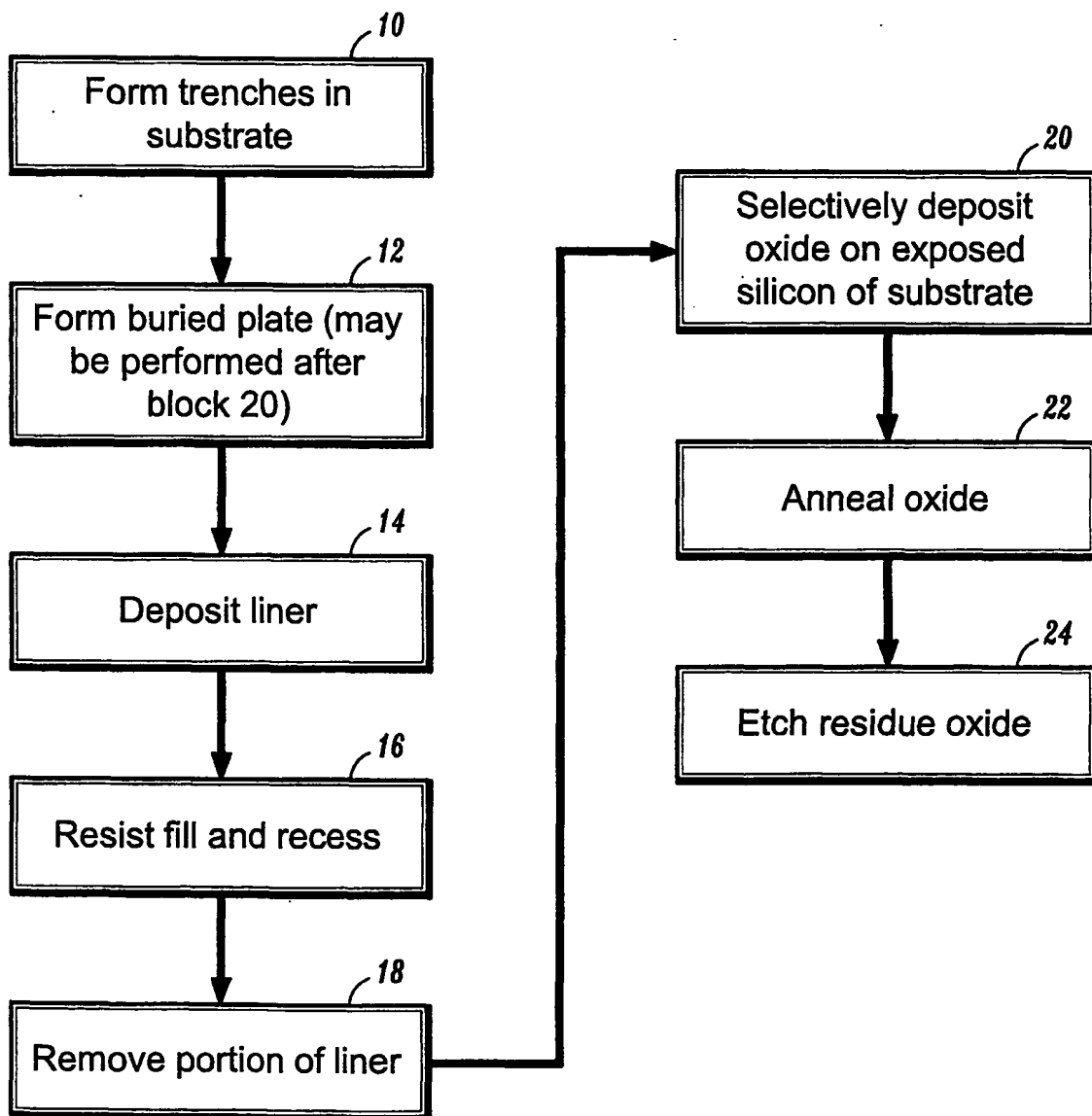
etching the nitride liner to a top level of the resist in the trench to expose the portion of the substrate in the trench.

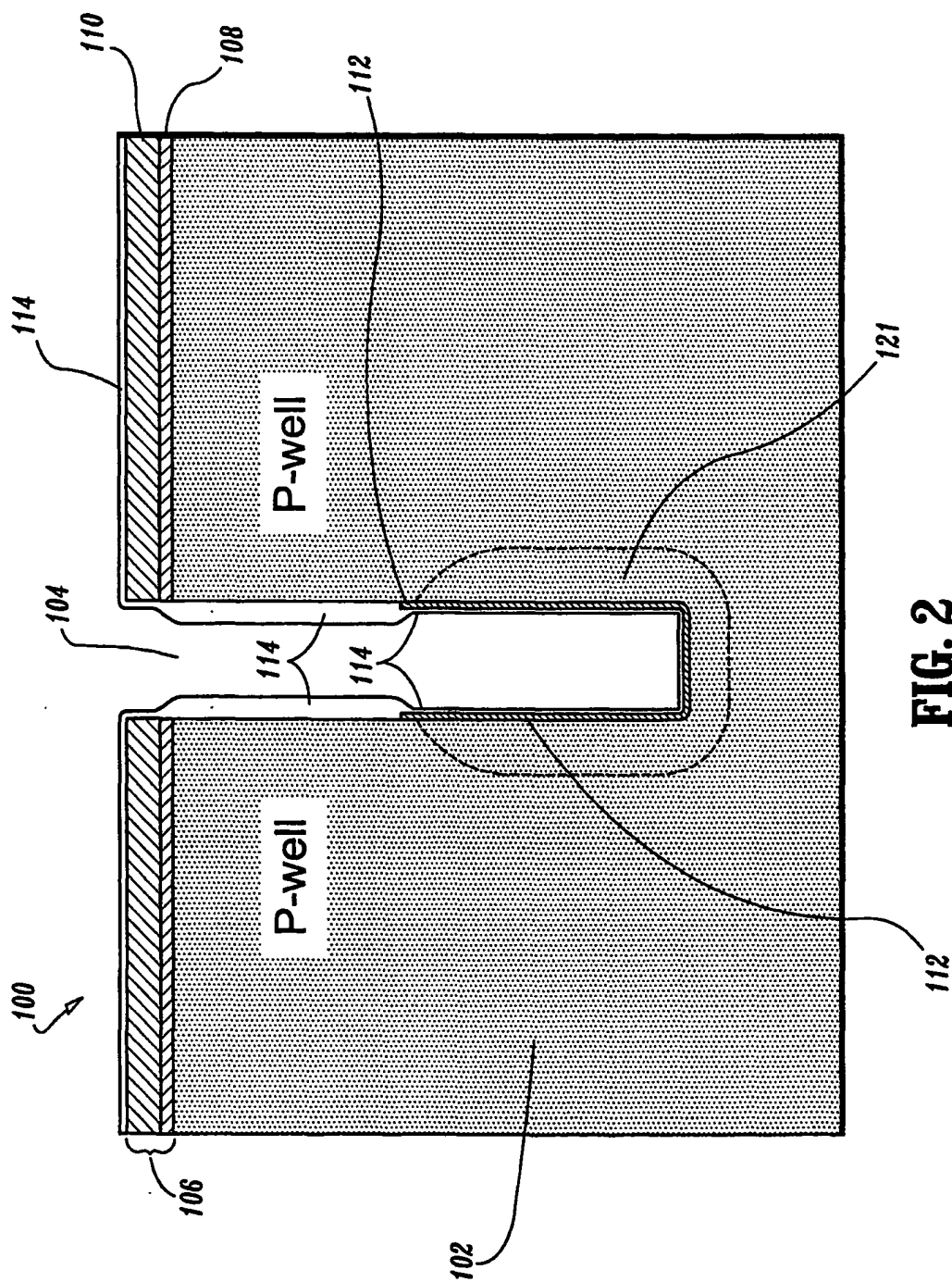
13. The method as recited in claim 9, wherein the nitride liner is between about 2 nm and 3 nm in thickness.

14. The method as recited in claim 9, further comprising the step of forming a buried plate adjacent to a lower portion of the trench.

15. The method as recited in claim 9, further comprising the step of annealing the oxide.

1/3

**FIG. 1**



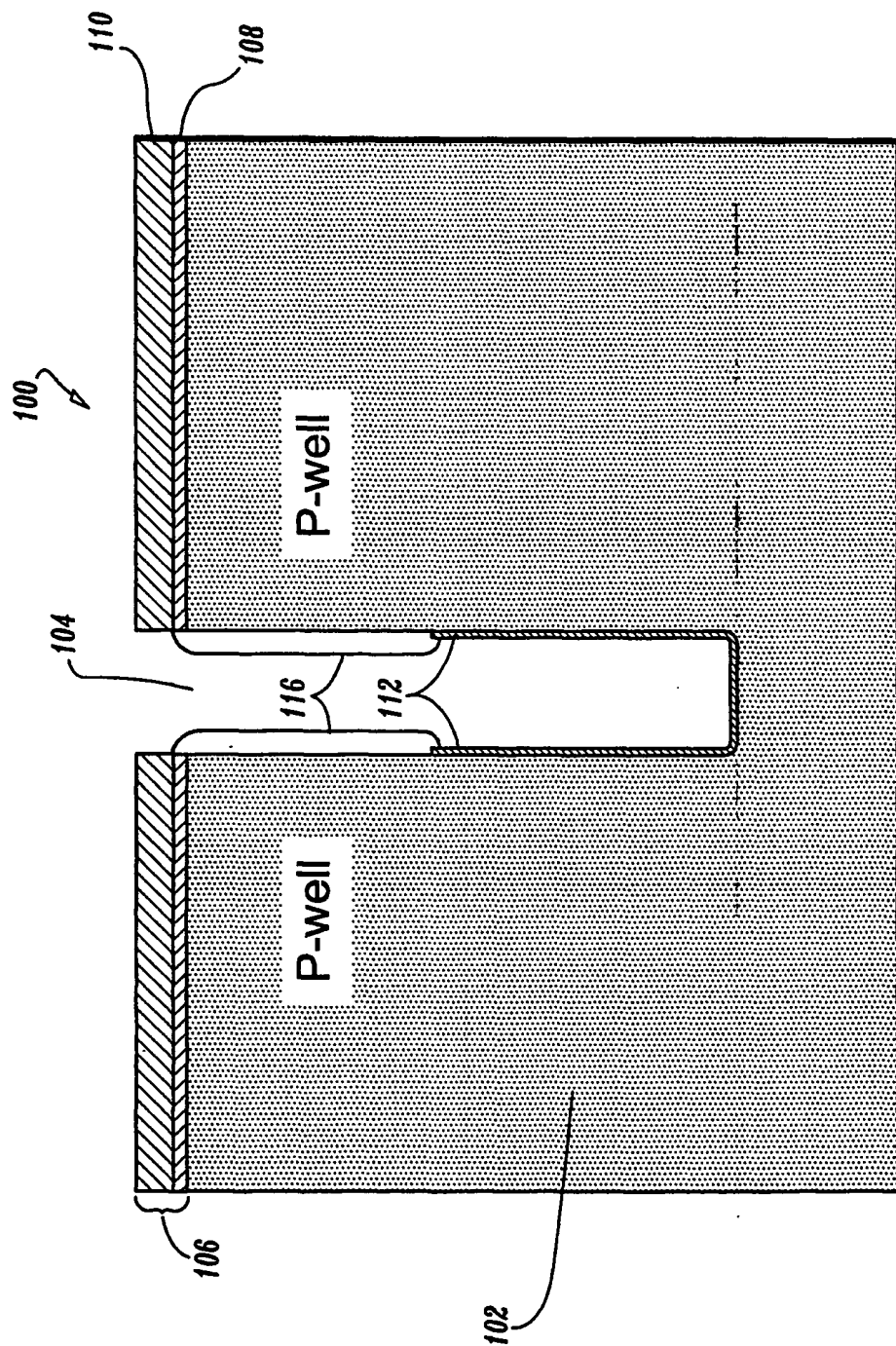


FIG. 3

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
27 December 2001 (27.12.2001)

PCT

(10) International Publication Number
WO 01/099158 A3

(51) International Patent Classification: H01L 21/8242

SPINDLER, Oswald; Lortzingstrasse 16, 85591 Vaterstetten (DE). GABRIC, Zvonimir; Herzog-Rudolf Weg 25, 85604 Zorneding (DE).

(21) International Application Number: PCT/US01/19578

(22) International Filing Date: 19 June 2001 (19.06.2001)

(74) Agents: BRADEN, Stanton, C. et al.; Siemens Corporation, Intellectual Property Dept., 186 Wood Avenue South, Iselin, NJ 08830 (US).

(25) Filing Language: English

(81) Designated States (national): JP, KR.

(26) Publication Language: English

(84) Designated States (regional): European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR).

(30) Priority Data:
09/596,606 19 June 2000 (19.06.2000) US

Published:
— with international search report

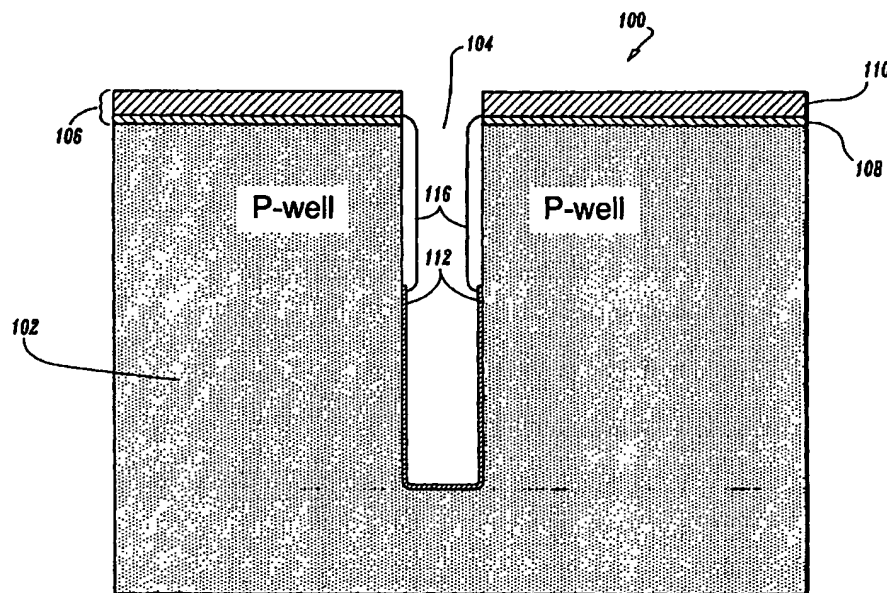
(71) Applicant: INFINEON TECHNOLOGIES NORTH AMERICA CORP. [US/US]; 1730 North First Street, San Jose, CA 95112-4508 (US).

(88) Date of publication of the international search report:
19 September 2002

(72) Inventors: BEINTNER, Jochen; 27 Clapp Avenue, Wappingers Falls, NY 12590 (US). MICHAELIS, Alexander; Grundermuehlenweg 38, 51381 Leverkusen (DE). GRUENING, Ulrike; Raintalerstr. 36, 81539 Munich (DE).

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: COLLAR FORMATION BY SELECTIVE OXIDE DEPOSITION



(57) Abstract: A method for forming an oxide collar in a trench, in accordance with the present invention, includes forming a trench (104) in a silicon substrate (102), and depositing and recessing a nitride liner (112) in the trench to expose a portion of the silicon substrate on sidewalls of the trench. An oxide (116) is deposited selective to the nitride liner on the portion of the silicon substrate. Residue oxide is removed from surfaces of the nitride liner to form a collar (116) in the trench.



WO 01/099158 A3

INTERNATIONAL SEARCH REPORT

International Application No

PCT/US 01/19578

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/8242

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 987 754 A (SIEMENS AG) 22 March 2000 (2000-03-22) column 22, line 19 -column 23, line 25; figure 4	1-15
P,X	EP 1 026 740 A (INFINEON TECHNOLOGIES CORP) 9 August 2000 (2000-08-09) column 5, line 22 - line 40; figures column 8, line 44 - line 56	1-15
A	US 5 399 389 A (SIEMENS AG) 21 March 1995 (1995-03-21) the whole document	1-15
	-/--	

☒ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

* Special categories of cited documents:

- *A* document defining the general state of the art which is not considered to be of particular relevance
- *E* earlier document but published on or after the international filing date
- *L* document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
- *O* document referring to an oral disclosure, use, exhibition or other means
- *P* document published prior to the international filing date but later than the priority date claimed

- *T* later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
- *X* document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
- *Y* document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.
- *G* document member of the same patent family

Date of the actual completion of the international search

6 December 2001

Date of mailing of the international search report

13/12/2001

Name and mailing address of the ISA

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040, Tx. 31 651 epo nl,
Fax: (+31-70) 340-3016

Authorized officer

Sinemus, M

INTERNATIONAL SEARCH REPORT

International Application No

PCT/US 01/19578

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	<p>ELBEL ET AL: "A new STI process based on selective oxide deposition Yfor CMOS logic" , VLSI TECHNOLOGY, 1998. DIGEST OF TECHNICAL PAPERS. 1998 SYMPOSIUM ON HONOLULU, HI, USA 9-11 JUNE 1998, NEW YORK, NY, USA, IEEE, US, PAGE(S) 208-209 XP010291189 ISBN: 0-7803-4770-6 the whole document</p> <p>-----</p>	1-15

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No

PCT/US 01/19578

Patent document cited in search report		Publication date	Patent family member(s)	Publication date
EP 0987754	A	22-03-2000	DE 19842665 A1	06-04-2000
			EP 0987754 A2	22-03-2000
			TW 441032 B	16-06-2001
			US 6200873 B1	13-03-2001
<hr/>				
EP 1026740	A	09-08-2000	US 6184091 B1	06-02-2001
			CN 1263358 A	16-08-2000
			EP 1026740 A2	09-08-2000
			JP 2000223668 A	11-08-2000
			US 6177698 B1	23-01-2001
<hr/>				
US 5399389	A	21-03-1995	EP 0582724 A1	16-02-1994
			JP 6168938 A	14-06-1994
<hr/>				